

FORM PTO 1449 (modified)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICELIST OF REFERENCES CITED BY APPLICANT(S)
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Attorney Docket No.

016887-1102

SERIAL NO.

Unassigned

10/804094

APPLICANT

Tomoharu TANAKA et al.

FILING DATE:

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GROUP: 2824

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
ju	A1	4,755,970	7/5/88	SCHRENK	365	201	
	A2	4,758,988	7/19/88	KUO	365	189	
	A3	4,763,305	8/9/88	KUO	365	200	
	A4	4,811,294	3/7/89	KOBAYASHI et al.	365	189	
	A5	4,881,200	11/14/89	URAI	365	189.04	
	A6	4,937,787	6/26/90	KOBATAKE	365	94	
	A7	4,943,948	7/24/90	MORTON et al.	365	201	
	A8	4,972,372	11/20/90	UENO	365	201	
	A9	5,077,691	12/31/91	HADDAD et al.	365	218	
	A10	5,086,413	2/4/92	TSUBOI et al.	365	230.01	
	A11	5,109,257	4/28/92	KONDO	357	23.5	
	A12	5,109,359	4/28/92	SAKAKIBARA et al.	365	189.07	
ju	A13	5,124,945	8/23/92	SCHRECK	365	185	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES/NO/ OR ABSTRACT

OTHER DOCUMENT(S) (Including Author, Title, Date, Pertinent Pages, Etc.)

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U.S. PATENT DOCUMENTS

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ju	A14	5,134,583	7/28/92	MATSUO et al.	365	200	
	A15	5,136,544	8/4/92	ROZMAN et al.	365	201	
	A16	5,142,496	8/25/92	VAN BUSKIRK	365	201	
	A17	5,148,398	9/15/92	KOHNO	365	201	
	A18	5,153,880	10/6/92	OWEN et al.	371	10.2	
	A19	5,163,021	11/10/92	MEHROTRA et al.	365	185	
	A20	5,172,339	12/15/92	NOGUCHI et al.	365	201	
	A21	5,299,162	3/29/94	KIM et al.	365	201	
	A22	5,355,340	10/11/94	COKER et al.	365	200	
	A23	5,361,277	11/1/94	GROVER	375	107	
	A24	5,428,571	6/27/95	ATSUMI et al.	365	189.05	
ju	A25	5,483,484	1/9/96	ENDO et al.	365	185.18	

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JK	A26	5,513,333	4/30/96	KYNETT et al.	395	430	
	A27	5,537,350	7/16/96	LARSEN et al.	365	185.330	
	A28	5,566,105	10/15/96	TANAKA et al.	365	185.22	
	A29	5,574,684	11/12/96	TOMOEDA	365	185.04	
	A30	5,574,688	11/12/96	McCLURE et al.	365	200	
	A31	4,597,062	06/24/86	ASANO et al	365	201	
	A32	4,819,212	04/04/89	NAKAI et al	365	230	
	A33	4,858,192	08/15/89	TATSUMI et al	365	200	
	A34	4,879,689	11/07/89	ATSUMI et al	365	201	
	A35	4,881,202	11/14/89	TSUJIMOTO et al	365	200	
	A36	5,025,418	06/18/91	ASOH	365	200	
	A37	5,126,973	06/1992	GARCIA ET AL.	365	200	
JK	A38	5,233,610	08/1993	NAKAYAMA	365	200	

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gu	A39	4,279,024	07/1981	SCHRENK	365	203	
	A40	5,172,338	12/1992	MEHROTRA	365	185	
	A41	5,434,819	07/1995	MATSUO et al.	365	189.07	
gu	A42	5,343,437	08/1994	JOHNSON et al.	365	230.3	

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gu	A43	3-259499	11/91	JAPAN	—	—	
	A44	4-82090	03/92	JAPAN	—	—	
	A45	62-188100	08/87	JAPAN	—	—	
	A46	4-82091	03/92	JAPAN	—	—	
	A47	2029145	03/80	GREAT-BRITAIN	—	—	
	A48	WO 90/12400	10/1990	WIPO	—	—	
gu	A49	41 10 371	10/1991	FED. REP. OF GERMANY	—	—	

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gu	A50		M. Momodomi et al, A 4-Mb NAND EEPROM with Tight Programmed V _t Distribution, IEEE Journal of Solid-State Circuits, vol. 28, no. 4, April 1991, pp. 492-495
gu	A51		Patent Abstracts of Japan, vol. 14, no. 381, 16 August 1990, p. 1093.

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INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>				APPLICANT Tomoharu TANAKA et al.				
				FILING DATE Concurrently Herewith		GROUP ART UNIT 2824		
U.S. PATENT DOCUMENTS								
EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB- CLASS	FILING DATE IF APPROPRIATE	
<u>Qu</u>	A52	4,794,564	12-27-1988	WATANABE	—	—		
	A53	5,297,096	03-22-1994	TERADA ET AL.	—	—		
	A54	5,357,462	10-18-1994	TANAKA ET AL.	—	—		
	A55	5,379,256	01-03-1995	TANAKA ET AL.	—	—		
	A56	5,544,117	08-06-1996	NAKAYAMA ET AL.	—	—		
	A57	3,917,933	11-04-1975	SCHEUNEMAN ET AL.	—	—		
	A58	4,456,995	06-26-1984	RYAN	—	—		
	A59	4,937,830	06-26-1990	KAWASHIMA ET AL.	—	—		
	A60	4,958,352	09-18-1990	NOGUCHI ET AL.	—	—		
	A61	5,452,311	09-19-1995	WELLS ET AL.	—	—		
	A62	4,980,888	12-25-1990	BRUCE ET AL.	—	—		
	A63	5,657,270	08-12-1997	OHUCHI ET AL.	—	—		
	A64	5,436,913	07-25-1995	YAMAMURA ET AL.	—	—		
	A65	4,460,982	07-17-1984	GEE ET AL.	—	—		
<u>Qu</u>	A66	5,321,699	06-14-1994	ENDOH ET AL.	—	—		
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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB- CLASS	TRANSLATION	
							YES	NO
<u>Qu</u>	A67	59-110096 A	06-25-1984	JAPAN	—	—	X	
<u>Qu</u>	A68	2-142000 A	05-31-1990	JAPAN	—	—	X	
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)								
<u>Qu</u>	A69	K. Arimoto et al., "A Speed-Enhanced DRAM Array Architecture with Embedded ECC", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 11-17.						
<u>Qu</u>	A70	K. Kobayashi et al., "A High-Speed Parallel Sensing Architecture for Multi-Megabit Flash E ² PROM's", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 79-83.						
<u>Qu</u>	A71	M. Momodomi et al., "An Experimental 4-Mbit CMOS EEPROM with a NAND-Structured Cell", IEEE Journal of Solid-State Circuits, Vol. 24, No. 5, Oct. 1989, pages 1238-1243.						
<u>Qu</u>	A72	M. Momodomi et al., "A High Density NAND EEPROM with Block-Page Programming for Microcomputer Applications", Proceedings of the IEEE 1989 Custom Integrated Circuits Conference, May 15-18, 1989, pages 10.1.1-10.1.4.						
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<i>ju</i>	A73	T. Tanaka, et al., "A Quick Intelligent Program Architecture for 3V-only NAND-EEPROMs", 1992 Symposium on VLSI Circuits, Digest of Technical Papers, pages 20-21.					
	A74	M. Asakura et al., "An Experimental 1-Mbit Cache DRAM with ECC", IEEE Journal of Solid-State Circuits, Vol. 25, No. 1, Feb. 1990, pages 5-10.					
	A75	R. Vancu et al., "Section 4: Nonvolatile and Fast Static Memories: A 35 ns 256k CMOS EEPROM with Error Correcting Circuitry", 1990 IEEE International Solid-State Circuits Conference, Digest of Technical Papers, Feb. 1990, pages 64-65					
	A76	Lexar Media, Inc.'s Corrected Answer to Toshiba corporation's Amended Complaint for Patent Infringement, Case No. C03-00167 CRB, March 5, 2003, pages 1-13.					
	A77	Lexar Media's Amended Patent Local Rules 3-3 and 3-4 Disclosures, Case No. C03-00167, October 16, 2003, pages 1-33 with Exhibits A-I.					
<i>ju</i>	A78	C.L. Chen et al., "Error-Correcting Codes for Semiconductor memory Applications: A State-of-the-Art Review", IBM J. Res. Develop., Vol. 28, No. 2, March 1984, pages 124-134.					
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